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Jupiter SE880 Hardware User Guide

1VV0301032 Rev.0 – 2012-10-31

http://www.sensorexpert.com.cn 400-883-3391

Making machines talk.

APPLICABILITY TABLE

PRODUCT
Jupiter SE880

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1. Introduction

1.1. Scope

This document describes the hardware features of the world smallest, high performance turnkey Telit GPS solution Jupiter SE880. Advanced 3D-System-in-Package embedded die technology is used to integrate SAW filter and most passive components. Recommendations are provided for integrating this receiver into customer designs requiring only a 32 KHz external crystal for its time-base and TCXO to complete the design, along with antenna, power and data connections adequate to the integrator's needs.

Features include class-leading sensitivity stability particularly at the extremes of -40 and +85°C, one-satellite acquisition of UTC, micro-power stand-by mode, innovative multi-filter RF architecture, CW jamming-resistant DSP, and super small size. This compact and powerful GPS SiP is in a 4.7 x 4.7 x 1.4 mm 34 pins LGA package.

1.2. Audience

This document is intended for helping GPS developers in the integration of the Telit Jupiter SE880.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

Alternatively, use:

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

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1.4. Document Organization

This document contains the following chapters:

"Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

"Chapter 2: "General Product Description" gives an overview of the features of the product.

"Chapter 3: "Specifications" provides in details the electrical characteristics of the product.

"Chapter 4: "Operation" explains the functions and features of the product.

"Chapter 5: "Applications and Schematic Examples" provides in details the hardware implementations of the product.

"Chapter 6: "PCB Layout" provides in details the PCB layout for design and manufacturing.

"Chapter 7: "Antenna" explains the antenna requirement of the product.

"Chapter 8: "Handling and Soldering" provides some handling recommendations that must be followed by customer in the manufacturing process.

"Chapter 9: "Safety Recommendation" provides some safety recommendations that must be follow by the customer in the design of the application that makes use of the SE880.

"Chapter 10: "Document History" provides the revision of this document.

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- Telit_Jupiter_SE880_Product Description

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2. General Product Description

The Telit's Jupiter SE880 is the world smallest, best-in-class turnkey GPS 3D-SiP navigation solution to combine off-the-die RF circuitries and most passives based on the CSR SiRFStarIV™ GPS PVT engine. The core of SE880 is state of the art GPS architecture employing spatially calibrated waveguide-quality radio paths inside the three-dimensional space of its architecture drastically reducing parasitic impedances characteristic of traditional 2-D RF designs. The SE880 is suitable for L1-band GPS and A-GPS systems to achieve best-in-class performance in all dimensions critical for regular or size-constrained GPS applications.

Jupiter SE880 is in 4.7 x 4.7 x 1.4 mm, 34 pins LGA package to make the chipset-versus-module decision an easy one to make for device integrators. SE880 chip size receiver module was conceived to shorten Time-to-Market and Integrators can attain a working SE880-based design in as little as a week versus several months when starting from a chipset reference design.

2.1. Features

High-performance Solution:

- Ultra high sensitivity frontend without the need of active antenna
- High-sensitivity navigation engine (PVT) tracks as low as -165dBm
- 48 track verification channels
- SBAS (WAAS, EGNOS, QZSS and others)

Adaptive Micropower Controller:

- Average of 50 to 500µA per hour to maintain hot start capability
- <10mW required for TricklePower mode

Three Stages Passive and Active Jammer Removal:

- Integrated pre-selection SAW filter at antenna port
- Integrated notch filter attenuates unwanted energy at 2.4GHz
- In-band jammers removal up to 80dB-Hz
- Tracks up to 8 CW jammers

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Advanced Navigation Features:

- 1-SV fast time sync for rapid UTC update
- Smart sensor I²C interface
- Embedded Data logger
- Measurement smoothing for pedestrians mode
- A-GPS (free 3-days CGEE and 14days SGEE; expandable to 31 days SGEE)

Simple To Use:

- Requiring only a 32 KHz crystal and TCXO along with antenna and power
- Typical solution on 2-layer PCB
- Optional external memory (SPI Flash or Serial EEPROM)
- Single 1.8V supply with integrated LDO and switcher mode
- GPIO Baud Rate and Protocol Configuration
- Fail safe I/O, including RTC and TCXO inputs
- Host I²C, SPI and UART supported

Mechanical Feature:

- Dimensions: 4.7 x 4.7 x 1.4 mm typ.
- Package: 34 pins LGA 0.4mm pitch
- Weight: 0.08g

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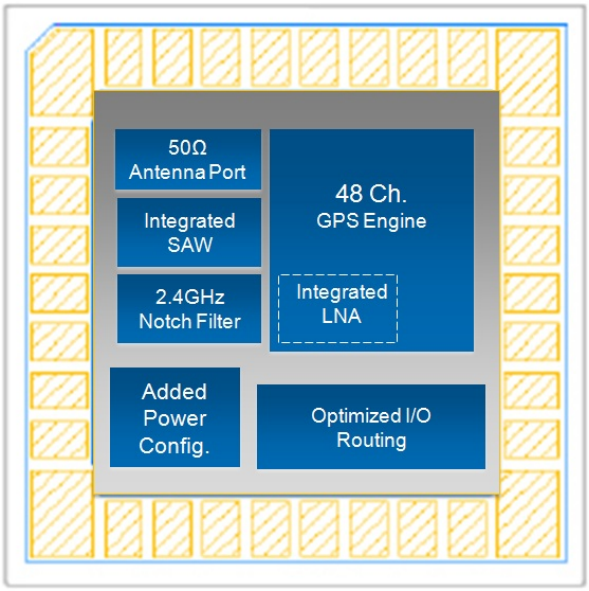
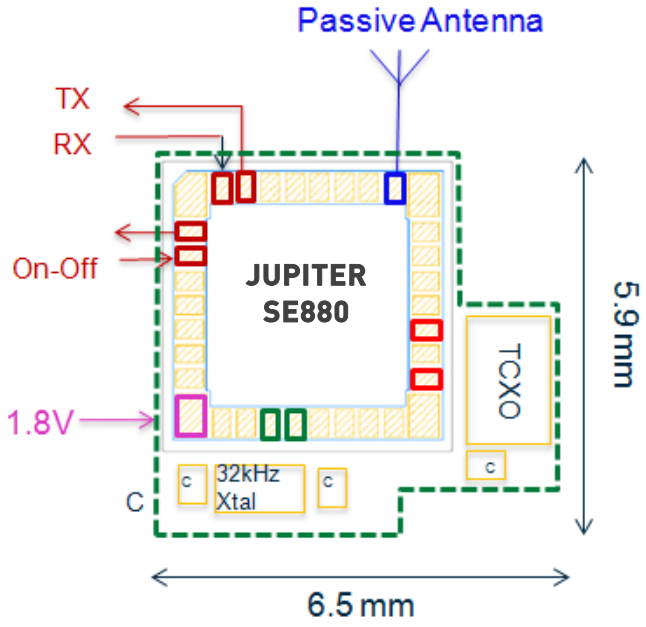
2.2. Block Diagram



2.3. Major Components



SE880 requires two external reference clocks (16.369MHz TCXO and 32.768kHz XTal), antenna and a 1.8V always ON supply with noise and ripple characteristics mentioned in Chapter 3 for reliable operation. This can be a 1.8V supply that is backed up by a very low current 1.8V LDO that will supply the 14uA typical when the GPS has been shut down into Hibernate mode.

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3. Specifications

3.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
RF Input Voltage	RF_In	3	V
RF Input power	RF_In	10	dBm
ESD Voltage (1)	RF_In	50	V
Main Supply Voltage	VDD	2.2	V
KA Voltage / I/O Supply Voltage	VKA	2.2	V
Core Supply Voltage	VBB_I	1.5	V
Input Pin Voltage	V_I	3.6	V
Output Pin Voltage	V_O	3.6	V
Storage Temperature	Tstg	-40 to 85	°C

WARNING : Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device.

ESD CAUTION:

Note (1): acc. to JESD22-A115A (machine model).

Apply ESD static handling precautions during manufacturing.

3.2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T	Operating temperature	-40	-	+85	°C
VDD	Supply voltage input	1.75	1.8	1.85	V
VDD_{AC}	Supply voltage ripple, AC coupled	-	-	54	mV (RMS) f=0.....3MHz
VDD_{AC}	Supply voltage ripple, AC coupled	-	-	15	mV (RMS) f > 3MHz

NOTE:

Noise management for a good GPS design is importance. Please obverse the stated VDD ripple requirement and apply appropriate regulated power source with proper filtering. SE880 EVK and reference design are typically built with Torex XC6221 1.8V LDO for the VDD supply.

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3.3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Current Usage					
I_{DD} (peak)	Supply current, peak acq.	-	47	70	mA
I_{DD} (ave)	Supply current average, tracking, LDO mode[(a)]	-	35	-	mA
I_{DD} (ave)	Supply current average, tracking, Switcher mode [(a)]	-	28	-	mA
I_{DD} (Hib)	Supply current, hibernate state	-	14	-	µA
I_{DD} (MPM)	Micro Power Mode average current	-	500	-	µA
Standard I/O					
V_{OL}	Low level output voltage, I_{OL} 2mA	-	-	0.4	V
V_{OH}	High level output voltage, I_{OH} 2mA	0.75*V DD	-	-	V
V_{IL}	Low level input voltage	-0.3	-	0.45	V
V_{IH}	High level input voltage, I_{OH} 2mA	0.7*V DD	-	3.6	V
R_{PU}	Internal pull-up resistor equivalent	50	86	157	kΩ
R_{PD}	Internal pull-down resistor equivalent	51	91	180	kΩ
L_I	Input leakage at Vl=1.8V or 0V	-10	-	10	µA
L_O	Tristate output leakage at V0=1.8V or 0V	-10	-	10	µA
C_I	Input capacitance, digital output	-	8	-	pF
Reference Clock Input					
TCXO_CLK	Reference clock input level (sine)	0.25	-	1.54	Vpk-pk
TCXO_CLK	Reference clock input level (square)	1.7	-	3.3	Vpk-pk

NOTE:

Note (a): This is only achieved if the software patch is in use. Please contact technical support for software patch applications. Without it, current consumption is approximately 5mA higher.

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3.4. System Specifications

GPS PVT Engine	
Receiver	GPS L1 C/A-code
Channels	48
TCXO	16.369MHz, 0.5ppm GPS TCXO (1.8V)
Real Time Clock	32.768KHz, Quartz Crystal, 12.5pF Load Capacitance
Sensitivity	
Tracking	-165 dBm
Navigation	-163 dBm
Re-acquisition(1)	-162 dBm
Acquisition	-148 dBm
TTFF (Time to First Fix)	
Hot Start(2)	<1 s typ.
Warm Start (2)	<33 s typ.
Cold Start at 34dB-Hz(2)	<36 s (90%)
Cold Start at 28dB-Hz(3)	<100s (99.73%)
Accuracy	
Horizontal Position Accuracy (4)	< 1.8m CEP50
Communication	
Host port configuration	UART, SPI or I2C configurable
Serial port protocol	NMEA-0183 rev. 3.0 (configurable to SiRF binary OSP)
Serial data format (UART)	8 bits, no parity, 1 stop bit
Baud Rate Detection	4800/9600/115200 baud configurable depending upon pull high or pull low with GPIO0 and GPIO1
Update rate (default)	1 Hz (configurable to 5Hz)

NOTE:

(1) SE880 is able to track satellites (no fix) at -165dBm and re-acquire position fix at -162dBm or C/No at 8.5dB-Hz or better; contact technical support for additional performance data.

(2) typical good view of sky, -137dBm or better.

(3) weak signal at -143dBm or better.

(4) 50% CEP, open-sky, 24hr Static.

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3.5. Pin out Description

Pad Number	Pad Name	Type	Description
1	GND1	PWR	GROUND for general
2	SYSTEM_ON	O	Indication that GPS is running (Active high)
3	ON_OFF	I	Input signal turns GPS ON or OFF (Active high pulse)
4	TM	O	1PPS time mark pulse
5	GND2	PWR	GROUND for general
6	VBB_I	PWR	Core digital supply 1.2V typ.
7	VREG_O	PWR	1.2V output of internal regulator
8	VKA	PWR	1.8v keep alive input for I/O and internal blocks
9	VDD	PWR	Main supply voltage, 1.8V (ALWAYS ON)
10	GPIO8	I/O	General Purpose Input/Output
11	GPIO3	I/O	General Purpose Input/Output
12	RTC_XI	CLK	RTC crystal or CMOS RTC clock input
13	RTC_XO	CLK	RTC crystal or open if no crystal
14	GPIO4	I/O	General Purpose Input/Output
15	GPIO2	I/O	General Purpose Input/Output
16	GPIO1	I/O	- Baud Rate and Protocol Detection - General Purpose Input/Output
17	GPIO0	I/O	- Baud Rate and Protocol Detection - General Purpose Input/Output
18	GND3	PWR	GROUND for general/TCXO
19	VCC_TCXO	PWR	TCXO voltage supply
20	GND4	PWR	GROUND for TCXO
21	TCXO_CLK	CLK	RF reference clock input; TCXO input or bare crystal output connection for built-in XO option
22	XTAL_CLK	CLK	Bare crystal input connection for built-in XO option or open for TCXO
23	GND5	RF	GROUND for antenna connection
24	GND6	RF	GROUND for antenna connection

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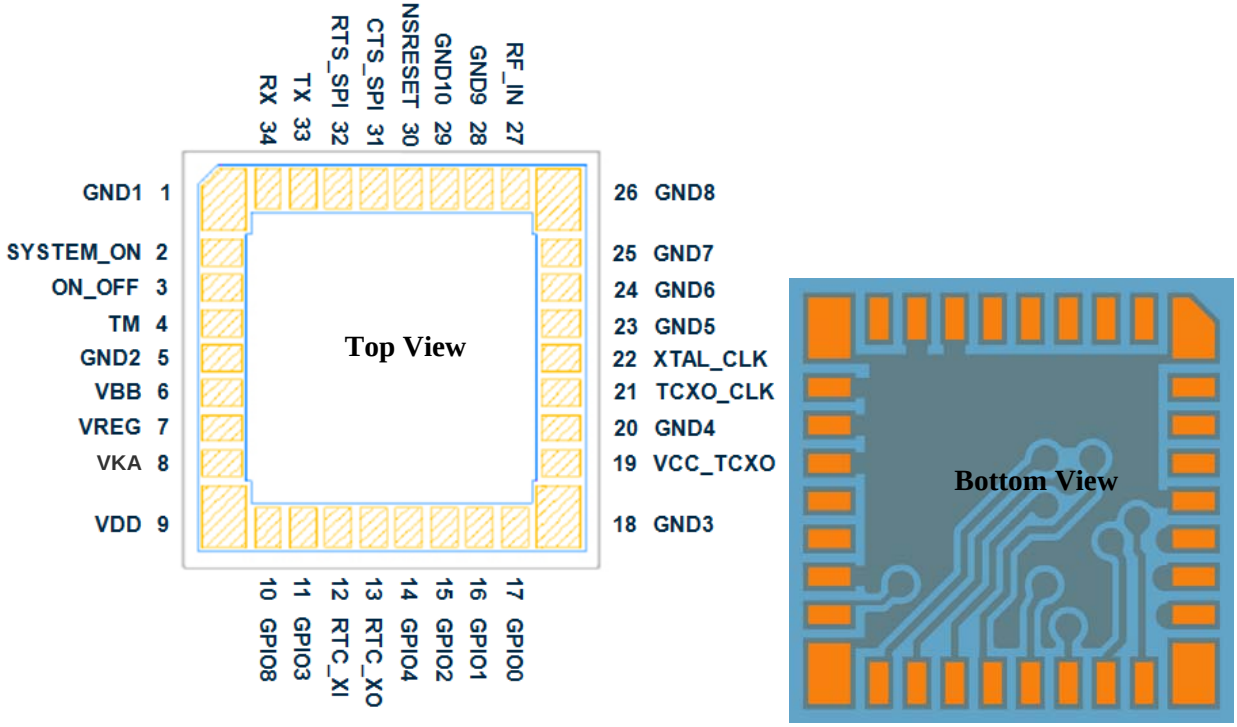
25	GND7	RF	GROUND for antenna connection
26	GND8	RF	GROUND for antenna connection
27	RF_IN	I	GPS RF Input (3V DC max rating)
28	GND9	RF	GROUND for antenna connection
29	GND10	RF	GROUND for antenna connection
30	NSRESET	I	GPS Reset (active low)
31	CTS_SPI	I/O	- Host port boot strap - General Purpose Input/Output
32	RTS_SPI	I/O	- Host port boot strap - General Purpose Input/Output
33	TX	O	UART/SPI/I2C (1.8V)
34	RX	I	UART/SPI/I2C (3.6V tolerant)



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3.6. Quality and Environmental Specifications

Test	Standard	Parameters
Preconditioning	JESD22-A113	24hr bake at 125°C; Moisture soak per MSL-3;Reflow 3X.
High Temperature Storage	JESD22-A103	+85°C ; 1008 hours .
Temperature Cycling	JESD22-A104	85°C (10 min)/-40°C (10 min); Transit time: 4s; Test cycles: 500 cycles.
Temperature Humidity Bias	JESD22-A101	+85°C, 85% R.H.;1008 hours

NOTE:

Moisture Sensitivity

Telit ships all devices dry packed with desiccant and moisture level indicator sealed in an airtight package. If on receiving the goods the moisture indicator is pink in color, then follow J-STD-033 "Handling and Use of Moisture/Reflow Sensitive Surface Mount Devices".

Storage (Out of Bag)

The SE880 meets MSL Level 3 – 168 hours Floor Life ≤ 30C / 60% RH. If the stated floor life expires prior to reflow process, then follow J-STD-033 "Handling and Use of Moisture/Reflow Sensitive Surface Mount Devices".

NOTE:

Production Control

The sensitivity of SE880 is less than 1 dB part to part variation.

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4. Operation

4.1. Operating modes

After power up the SE880 boots from the internal ROM to Hibernate state. The operation of SE880 requires ON_OFF interrupt to wake up for Normal (Navigation, Full on) mode.

Modes of operation:

- Full on (Navigation, Full Power)
  - Power management system modes

- Hibernate state

4.2. Full on mode

SE880 boots for internal 1.2V LDO regulator mode. Internal Switcher mode regulator reduces power consumption and requires a binary command from host to enable Switcher mode.

SE880 will enter Hibernate state after first power up with host port configuration and GPIO0 and GPIO1 settings. The Navigation mode will start after waking up from Hibernate state in cold start mode by sending ON_OFF signal interrupt pulse from host. This mode is also referenced as Full on, Full Power or Navigation mode.

Navigation is available and any configuration settings are valid as long as the VDD power supply is active. When the VDD is powered off, settings are reset to the configuration set at the host port and GPIO0 and GPIO1. Receiver performs a cold start on next power up.

VDD supply is intended to be kept active all the time and navigation activity is suggested to be controlled.

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4.2.1. Main Serial Interface Configuration

User can select the serial interface (host port) between UART, SPI (slave) or I^2C (master/slave) during power up boot depending upon how the CTS_SPI and RTS_SPI pins are strapped at power up. Either leave the pin floating, apply a 10K resistor to +1.8V (PU) or apply a 100K resistor to GND (PD).

Mode	CTS_SPI (internal pull-down)	RTS_SPI (internal pull-up)
UART	PU	Leave floating
I2C	Leave floating	PD
SPI	Leave floating	Leave floating

4.2.2. Baud / Protocol Selection

GPIO0 and GPIO1 can be used to configure the serial interface to output NMEA at standard baud rates. If SE880 is not using I²C or SPI flash devices on GPIO0 and GPIO1. The table below lists the settings for GPIO0 and GPIO1 to configure the baud rate at start-up.

GPIO0	GPIO1	Protocol	Baud Rate
Pull high	Pull high	NMEA	4800
Pull high	Pull low	NMEA	9600
Pull low	Pull high	NMEA	38400
Pull low	Pull low	OSP	115200

NOTE:

The default data format for UART: 8 data bits, no parity, 1 stop bit.

After start-up, the GPIOs can be released for other purposes.

This flexibility is not available if any MEMS or non-volatile memory devices are attached to the auxiliary serial bus. The internal software default baud rate is NMEA 4800 when an SPI Flash or EEPROM device is attached, but can be changed via a CCK patch or an OSP message.

Failure to tie GPIO0 and GPIO1 high or low in the absence of both SPI flash and EEPROM causes an increase in standby and hibernate current and also causes the start-up configuration of the UART to be indeterminate.

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4.2.3. NMEA Output Messages

NMEA v3.0 is the default protocol. The following messages are output by default:

- RMC = 1 second update
- GGA = 1 second update
- GSA = 1 second update
- GSV = 5 second update

Reference the NMEA protocol manual for additional message details.

4.2.4. SiRF OSP Output Messages

SiRF One Socket Protocol (OSP) is supported. This is an extension of the existing SiRF Binary protocol.

The following messages are output once per second:

- MID2
- MID4
- MID9
- MID41
- MID56, 5
- MID56, 35

Reference the SiRF One Socket Protocol manual for additional message details.

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4.2.5. Functions and Capabilities

Feature	Description	Availability
SBAS (WAAS, EGNOS, QZSS)	Improve position accuracy by using freely available satellite based correction services called SBAS (Satellite Based Augmentation System).	A
Low Signal Acquisition	Acquires satellites and continues navigating in extremely low signal environments.	Yes
Low Signal Tracking	Continues tracking in extremely low signal environments.	Yes
Time Mark Pulse (1PPS)	A timing pulse generated every second the receiver is in a valid navigation state (5 SVs required for initial pulse start-up).	Yes
MEMS	3-axis accelerometer support for static detection and wake-up. 3-axis magnetometer support for compass heading.	A
3 Day CGEE	AGPS using prediction of ephemeris from live (downloaded from satellites), ephemeris stored in memory.	Yes
14 Day SGEE	AGPS using server-generated extended ephemeris is now compatible with 14-day prediction files available from the Telit's server (expandable to 31 days). These files can be saved in SPI Flash, EEPROM or host memory.	A
Adaptive Jammer Detection	System scans for up to 8 CW jammers for removal by the GPS.	Yes
2.4GHz Notch Filter	System can reject 2.4GHz signals at the antenna port input up to 38dB attenuation.	Yes
1SV Fast Time-Sync	Determine UTC time quickly from one GPS satellite	A
Almanac Based Positioning	Allows fast cold starts TTFF 22 s. typ. based on factory set (or broadcast or pushed) Almanac data.	A
SPI Flash Support	Supports 4 Mb SST and EON SPI flash devices. SE880 uses flash memory for storage of almanac, EE, data logging, crystal and XO temperature models and patch code.	A
Data Logging	The embedded data logging function is configurable and will save data on SPI flash.	A
Baud/Protocol Selection	Baud rate and protocol selection can be set upon start up through GPIO0 and GPIO1 configuration.	Yes
Yes = always enabled	A = available, but not enabled by default	

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4.3. Power Management System Modes

SE880 supports different operating modes for reduced average power consumption like Adaptive TricklePower™, Micro Power modes, Push-to-Fix™ and Advanced Power Management.

1. *Adaptive Trickle Power* (ATP)

ATP is a duty-cycled mode. The system enters standby between navigation updates. This mode focuses on an update rate and navigation solution quality, so it can transition to Full Power Mode for 100ms to 800ms and provides a valid fix. This results in variable power savings but for a fixed output rate, much more reliable performance. Between fixes with 1 to 10 sec interval the receiver stays in Hibernate state. Applications using TP Mode perform similarly to applications using full power, but with significant power savings in strong-signal conditions. This mode is configurable with SiRF binary protocol message ID151. The receiver stays once in while in Full on power mode automatically to receive new ephemeris data, almanac data, ionospheric and UTC data, perform RTC convergence, or if received signal levels drop below certain level.

2. *Micro Power Mode* (MPM)

MPM is a very low-power maintenance mode. The objective of MPM is to remain below a stated average current level while maintaining a low level of uncertainty in time, frequency, position and ephemeris state. The receiver operates by capturing a buffer of GPS samples at infrequent intervals and analysing the data to update its time, frequency and position estimates. For satellites needing updated ephemeris data, a data collection is scheduled when strong signals are detected. During the data collection phase, time and frequency calibration operations are also carried out. Typical Capture/Update frequency varies: about once every ten minutes for 9 seconds. Data collection is twice an hour at ~18 seconds each. Rest of the time the receiver stays in Hibernate state and achieves 500µA typ. average current drain. The host wakes up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us) to perform a fix. After valid fix, operation can return back to MPM by re-sending the configuration binary message from host. This mode is configurable with SiRF OSP (One Socket Protocol) binary protocol message MID218.

3. *Push to Fix Mode* (PTF)

PTF Mode is for applications that require infrequent position reporting and average current levels are proportionally lower relative to ATP Mode duty-cycle. This mode allows the receiver to wake up periodically, typically every 30 minutes (configurable between 10 sec to 2 hours), for position update and to determine if a refresh of GPS time, ephemeris data and RTC calibration is required before the next HIBERNATE cycle. Rest of the time the receiver stays in Hibernate state. When position update is needed, the host can wake up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us). This mode is configurable with SiRF binary protocol message ID151 & 167.

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4. Hibernate state

Hibernate state means a low quiescent (14μA typ.) power shunt down state. TX and RX signals are configured to high input impedance state. In this state, only the RTC oscillator, clock monitor, RTC time counter, BBRAM are powered. The main supply input VDD shall be kept active all the time, even during Hibernate state. Operation is resumed by host interrupt at ON_OFF control input (rising edge toggle low-high-low >90us).

Hibernate state allows a Hot Start within 2-4 hours of last shut down. The GPS receiver must have had a valid fix with sufficient visible satellites before having been shut down via the ON-OFF line or serial command.

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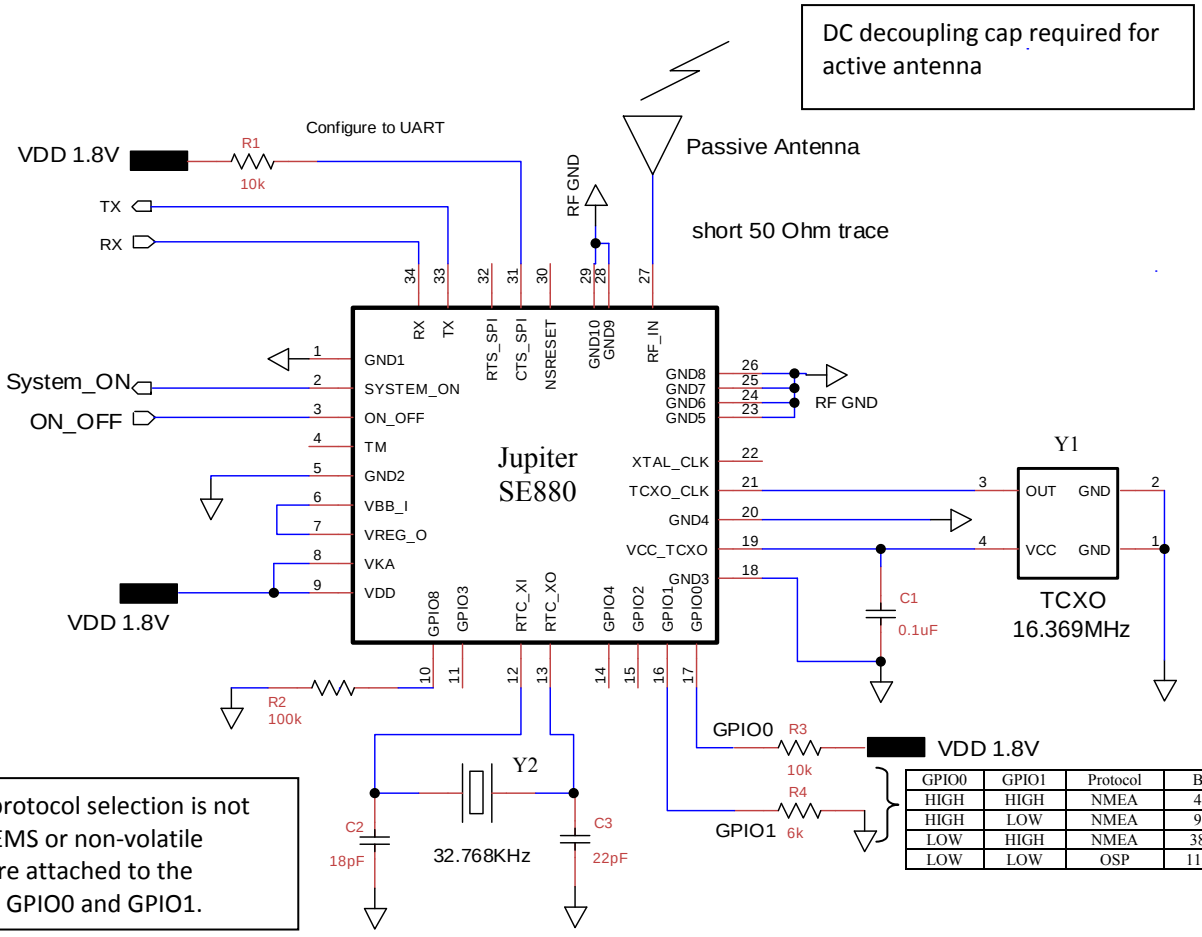
5. Applications and Schematic Examples

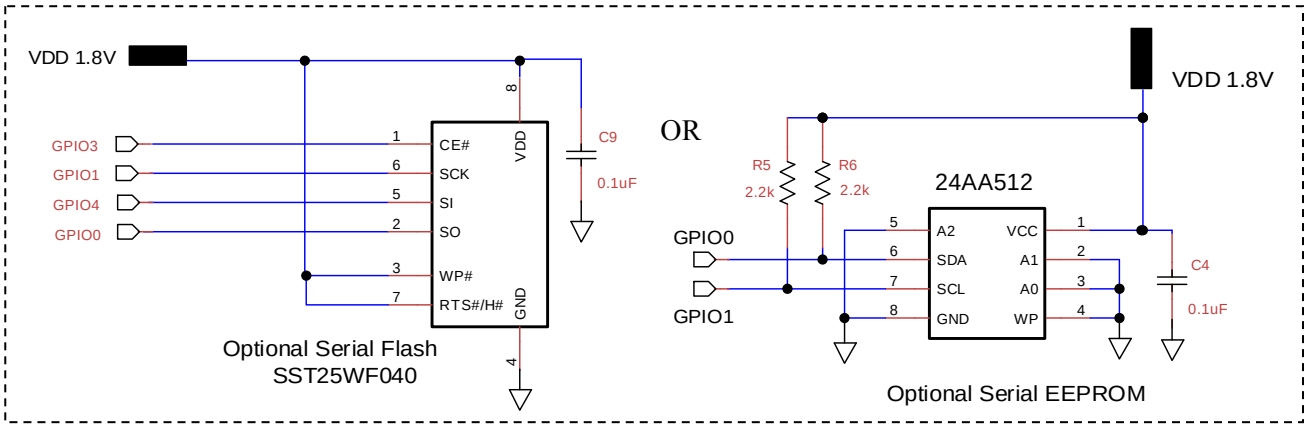
The circuit below shows a basic design for use with UART interface.

Power Management: LDO mode
Baud and Protocol Selection: NMEA 9600 Baud



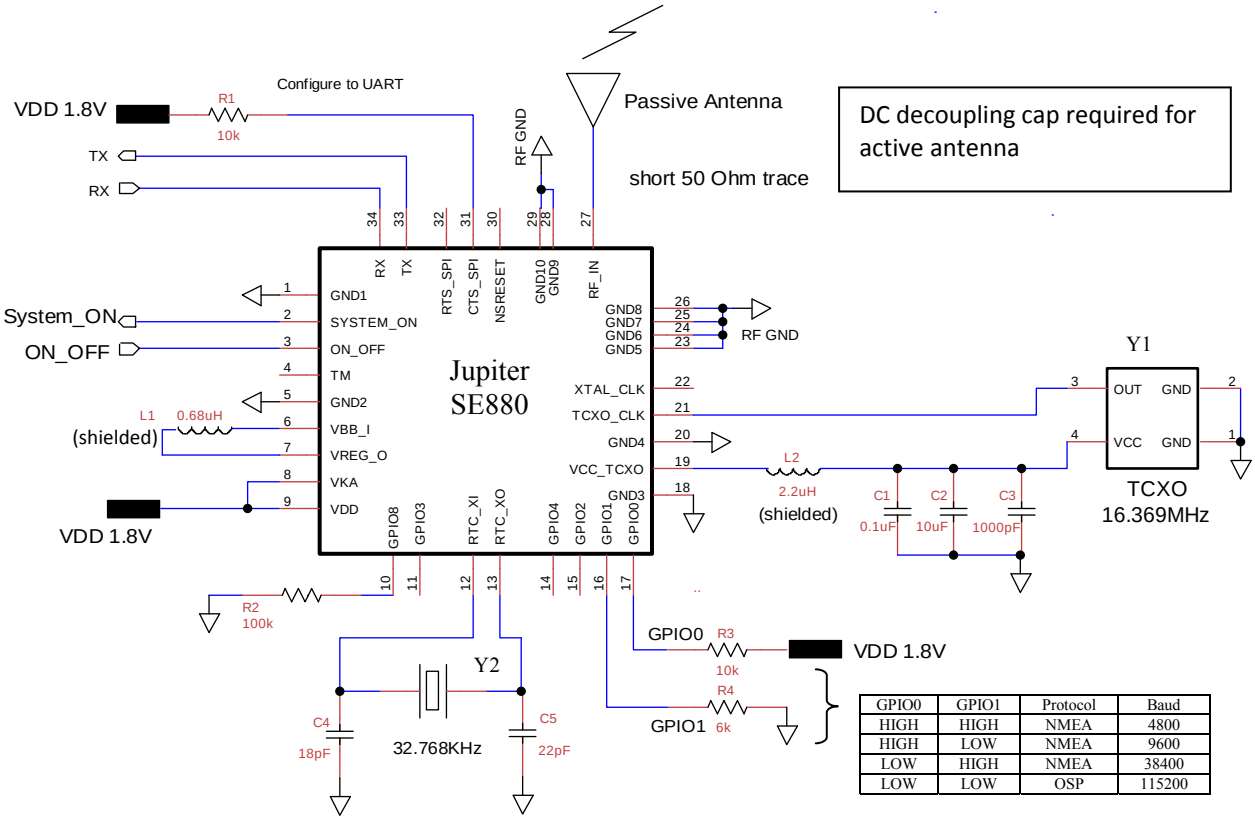
GPIO0	GPIO1	Protocol	Baud
HIGH	HIGH	NMEA	4800
HIGH	LOW	NMEA	9600
LOW	HIGH	NMEA	38400
LOW	LOW	OSP	115200

The flexibility for protocol selection is not available if any MEMS or non-volatile memory devices are attached to the auxiliary serial bus GPIO0 and GPIO1.

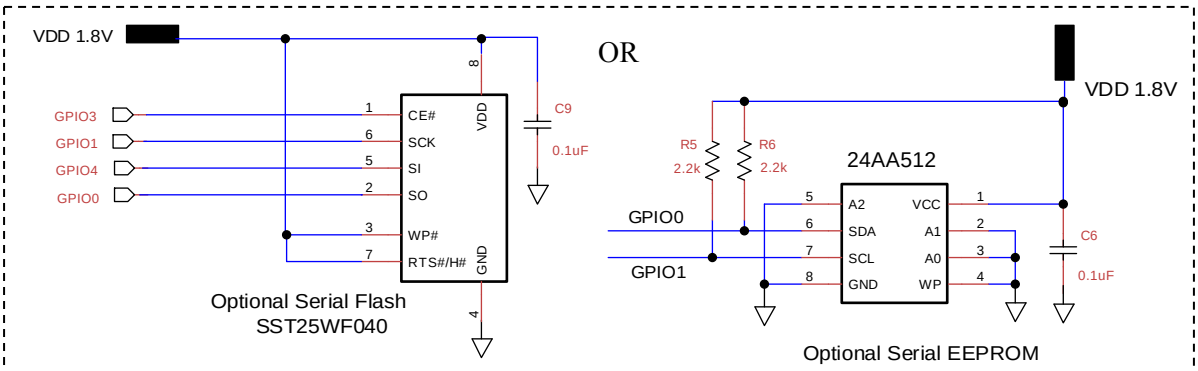


The circuit below shows a basic design for use with UART interface.

Power Management: Switcher mode
Baud and Protocol Selection: NMEA 9600 Baud



GPIO0	GPIO1	Protocol	Baud
HIGH	HIGH	NMEA	4800
HIGH	LOW	NMEA	9600
LOW	HIGH	NMEA	38400
LOW	LOW	OSP	115200



The flexibility for protocol selection is not available if any MEMS or non-volatile memory devices are attached to the auxiliary serial bus GPIO0

NOTE:

System noise is 2dB higher with switcher mode

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5.1. Bill of Material

Basic BOM for LDO Mode			
Designator	**Value**	**Description/Comments**	**Vendor**
Y1	16.369MHz	GPS TCXO, 0.5ppm, 1.8V	Rakon, NDK, Epson, Kyocera, Pericom, TXC
Y2	32.768KHz	RTC Quartz Crystal, 12.5pF load Cap	River, NDK and others
C1	0.1uF	Decoupling capacitor, place close to TCXO	-
C2	18pF	Loading capacitor	-
C3	22pF	Loading capacitor	-
R1	10k	Port configuration	-
R2	100k	Not used, pull-down	-
R3	10k	Baud/Protocol Selection	-
R4	6k	Baud/Protocol Selection	-

Basic BOM for Switcher Mode			
Designator	**Value**	**Description/Comments**	**Vendor**
Y1	16.369MHz	GPS TCXO, 0.5ppm, 1.8V	Rakon, NDK, Epson, Kyocera, Pericom, TXC
Y2	32.768KHz	RTC Quartz Crystal, 12.5pF load Cap	River, NDK and others
C1	0.1uF	Decoupling capacitor, place close to TCXO	-
C2	10uF	Low ESR decoupling capacitor, place close to TCXO	-
C3	1000pF	Decoupling capacitor, place close to TCXO	-
C4	18pF	Loading capacitor	
C5	22pF	Loading capacitor	
R1	10k	Port configuration	-
R2	100k	Not used, pull-down	-
R3	10k	Baud/Protocol Selection	-
R4	6k	Baud/Protocol Selection	-
L1	0.68uH	Shielded power inductor, EPL2010, switch mode regulator	CoilCraft
L2	2.2uH	Shielded power inductor, EPL2010, filtering	CoilCraft

NOTE:

Rakon TCXO IT2205APE 508303 and River TFX-04 RTC are used in reference design.

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5.2. External Memory

SE880 supports both SPI serial Flash and EEPROM for simultaneous storage of CGEE and SGEE (up to 31 days in length), ROM patch storage, and data logging feature (SPI Flash only). For detailed applications, please refer to application notes or contact technical support.

Vendor	Value	Description/Comments
SST	SST25WF040	SST 1.8V serial Flash memory 4Mbit
SST	24AA512	SST I^2C serial EEPROM 512Kbit

5.3. Power Supply

The SE880 requires only one VDD supply voltage of 1.8 volts. Rather than having a "split" power supply design of main and backup, the SE880 manages all of its power modes internally and VDD supply intended to be kept alive all the time.

First power up may take 300ms typ. due to internal RTC startup time after which the SE880 will enter into the lowest power "hibernate" state. Upon pulsing the ON_OFF signal, the SE880 will transition to the "operate" state. Pulsing the ON-OFF signal a second time will transition the SE880 back into the "hibernate" state.

The current power state of the SE880 can be determined by monitoring the "SYSTEM-ON" signal. A logic low indicates the module is in "hibernate", whereas logic high indicates the module is in "operate" state.

When power supply is intended to be removed, it is suggested to send the ON_OFF signal prior VDD removal for to send a serial message in NMEA format ($PSRF117,16*0B<CR><LF>) or binary (MID 205) to shut down firmware operations orderly. Otherwise e.g. external EEPROM may get corrupted if power down happens in the middle of EEPROM writing, which may increase in TTFF.

If the 1.8 volt VDD supply is removed from the SE880 (regardless of power state) it will lose current RTC time and will lose the contents of the internal SRAM. To prevent improper startup, once power is removed, keep the power removed for approximately 10 seconds so the internal SRAM contents can clear reliably.

If external memory or data storage at host memory is used and it is likely that power supply will be removed abruptly, suggestion is to monitor the 1.8 volt supply and issues an internal hardware reset (NSRESET to low state) if the supply drops below 1.7 volts. This reset protects the memory from accidental writes during a power down condition. However, the reset also clears the RTC time and forces the SE880 into a hibernate state.

To prevent this, the 1.8 volt supply must be regulated to be within ±50 mV of nominal voltage inclusive of load regulation and power supply noise and ripple. Noise and ripple outside of these limits can affect GPS sensitivity and also risk tripping the internal voltage supervisors, thereby shutting down the SE880 unexpectedly. Regulators with very good load regulation

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are strongly recommended along with adequate power supply filtering to prevent power supply glitches as the SE880 transitions between power states.

Aluminum electrolytic capacitors are not recommended at the input to the SE880 due to their high ESR. Low ESR ceramic capacitors are recommended with a minimum value of 10uF in parallel with a 0.1uF ceramic capacitor, but make sure the LDO is stable with such capacitors tied to the output.

As mentioned above, power supply voltage, noise and ripple must be between 1.75V and 1.85V for all frequencies up to 3MHz. Above 3MHz, the noise and ripple component must not exceed ±15mV. To help meet these requirements, a separate LDO for the SE880 is suggested.

NOTE:

SE880 EVK and reference design are typically built with Torex XC6221 1.8V LDO for the VDD supply.

5.4. Implementing Pseudo Battery Back-up

As mentioned above, the SE880 cannot tolerate removal of the 1.8 volt supply without losing RTC time and SRAM data. The main supply voltage can be switched to a backup supply external to the SE880 provided the receiver is allowed time to enter the hibernate state. This can be accomplished by monitoring the status of the SYSTEM-ON line, which will be low whenever the SE880 is in the hibernate state. At this point, the main supply can be safely switched over to the backup supply provided the 1.8 volt supply stays within specification. Similarly, the switch back to the main supply must occur prior to placing the SE880 into full power mode.

If the product containing the SE880 needs to support abrupt removal of power, then the module will require a split rail design for the VDD power. Please refer to application notes or contact technical support for details.

5.5. Understanding ON-OFF and SYSTEM-ON

The SE880 power is controlled by a state machine. This state machine is clocked by the internal 32 KHz RTC clock, and is controlled by internal signals as well as the ON_OFF and NSRESET signals. The SYSTEM_ON signal reflects the power state of the SE880, logic low for hibernate mode, and logic high for full power mode.

When power is first applied, the internal RTC must start up before the state machine can begin operating. ON_OFF signals applied before the state machine is ready for them will be ignored. The SE880 signals the readiness to accept ON-OFF signals by outputting a pulse on the SYSTEM_ON line after power is first applied. This pulse is only output upon application of power, and is not output when the receiver is in hibernate or full power mode.

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The ON_OFF signal is normally low. When it transitions high, it should stay high for a time equivalent to a minimum of 3 RTC clock cycles (90µs). The signal may then transition low and remain low until the next change in power state is desired.

The SE880 powers up directly into the hibernate state. It is possible to have the module automatically transition to the full power state by tying the SYSTEM_ON output to the ON_OFF input. GPIO8 should also be tied high, which changes the ON_OFF signal to just an ON signal. However, this implementation eliminates the possibility of using the ON_OFF signal to change power states. If the serial command to place the SE880 in hibernate mode is issued, the receiver will transition to the hibernate state with no way other than removal and reapplication of power (with resulting RTC and SRAM data loss) to force the receiver to power up. For some users, this may be all that is required if time and data retention are not important during a power down situation.

A single OR gate with one input being SYSTEM_ON and the other being an external pulse will allow the receiver to be turned back on with a suitable pulse, but it will not be possible to use a second pulse as it is blocked with the SYSTEM_ON signal. The only option to place the receiver in hibernate state is to issue the serial command.

If full ON_OFF control is desired along with having SYSTEM_ON auto-start the receiver, then additional logic is needed to detect the first falling edge of SYSTEM_ON and using this detection to gate off the SYSTEM_ON signal to the ON-OFF signal.

If GPIO8 is pulled to logic 1, then the ON_OFF input is modified to be just an ON input. It would not be possible to place the SE880 into hibernate by pulsing ON-OFF in this case. This feature could be useful by inverting the RX input and applying it to the ON_OFF input, thus causing the receiver to enter full power mode when a serial message is received. Of course, the first message would not be processed as the receiver has not fully woken up.

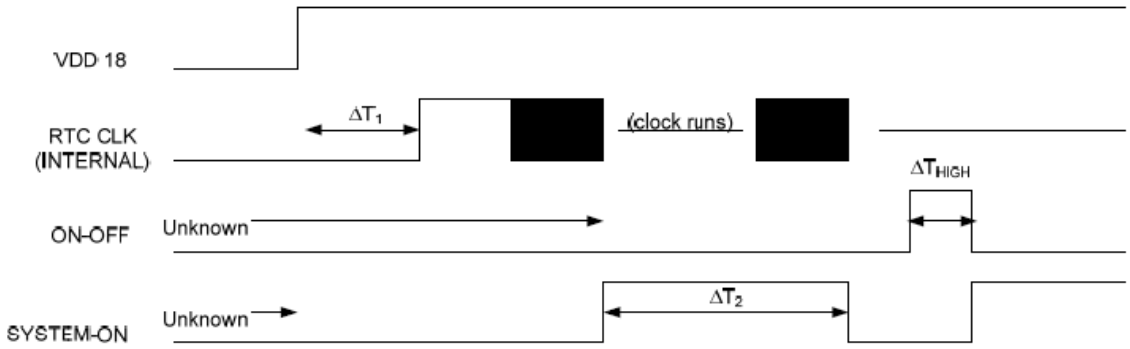

Figure 1 – Initial Application of Main Power

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Timed Parameter	Prior Event/State	Symbol	Min	Typ	Max	Unit
RTC startup time	First power applied	Δ T1	0	299	1000	ms
FSM Ready pulse	RTC running	Δ T2	10			TRTC
Min ON-OFF high		Δ THIGH	3			TRTC
TRTC is equivalent to one RTC (32.678KHz) clock cycle.						

5.6. Reset Design Details

The SE880 will generate an internal reset as appropriate. No external reset signal needs to be applied. When power supply VDD may be abruptly removed, suggestion is to use externally generated reset by means of monitor the 1.8 volt supply and issues an internal hardware reset (NSRESET to low state) if the supply drops below 1.7 volts.

If an external reset is desired, the signal must be either open collector or open drain without any form of pullup. Do not pull this line high with either a pullup or a driven logic one. When this line is pulled low, the SE880 will immediately drop into hibernate mode with some loss of data. When the external reset is released, the SE880 will go through its normal power up sequence provided the VDD supply is within specifications.

5.7. Main Serial Interface

The SE880 has the capability to operate in serial UART mode, SPI mode or I^2C mode depending upon how the CTS_SPI and RTS_SPI pins are strapped at power up. Either leave the pin floating, apply a 10K resistor to +1.8V (PU) or apply a 100K resistor to GND (PD).

Mode	CTS_SPI (internal pull-down)	RTS_SPI (internal pull-up)
UART	PU	Leave floating
I^2C	Leave floating	PD
SPI	Leave floating	Leave floating

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5.7.1. UART Mode

The CTS_SPI pin should be pulled high through a 10K resistor to the 1.8 volt supply. The RTS_SPI pin can be left open or pulled high. Upon power up, the SE880 will communicate using a standard asynchronous 8 bit protocol with messages appearing on the TX line, and commands and data being entered on the RX line. Note the CTS_SPI and RTS_SPI lines are read at power up or reset only and are not used afterwards. In particular, no flow control operations are performed.

5.7.2. I²C Mode

The RTS_SPI pin should be pulled low through a 100K resistor to GND. The CTS_SPI pin can be left open or pulled low. Upon power, the SE880 acts as a master transmitter and a slave receiver. Pull-ups to a 1.8V to 3.6V power supply in the range of 1K to 2.2K are required on the RXA and TXA lines when used in I²C mode. In this mode, the pins are defined below:

Signal Name	I²C Function
RX	I²C Bus Data (SDA)
TX	I²C Bus Clock (SCL)

Bit rates to 400K are achievable. Note the CTS_SPI and RTS_SPI lines are read at power up or reset only and are not used afterwards.

The operation of the I²C with a master transmit and slave receive mimics a UART operation, where both SE880 and host can independently freely transmit. It is possible to enable the master transmit and slave receive at the same time, as the I²C bus allows for contention resolution between SE880 and a host vying for the bus.

NOTE:

This I²C port should not be confused with the secondary I²C port on the SE880 which is reserved for external serial EEPROM, Serial Flash and MEMS sensors.

The I²C host port interface supports:

- Individual transmit and receive FIFO lengths of 64B
- The default I2C address values are:
  - Rx: 0x60
  - Tx: 0x62
- Operating mode is multi-master:
  - Transmit side operates as a master by seizing the I²C bus when detected idle
  - Receive side operates as a slave when another master seizes bus and transmits to our address

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5.7.3. SPI Mode

If both the CTS_SPI and RTS_SPI pins are left floating, the SE880 will power up in slave SPI mode, supporting both SPI and Microwire formats. In this mode, the four pins are defined below:

Signal Name	SPI Function
RTS_SPI	SSPI_SS_N slave SPI chip select (CS#) active low
CTS_SPI	SSPI_CLK slave SPI clock input (CLK)
RX	SSPI_DI slave SPI Data inputt (MOSI)
TX	SSPI_DO slave SPI data output (MISO)

The host interface SPI is a slave mode SPI:

- An interrupt is provided when the transmit FIFO and output serial register (SR) are both empty
- The transmitter and receiver each have independent 1024B FIFO buffers
- The transmitter and receiver have individual software-defined 2-byte idle patterns of 0xa7 0xb4
- SPI detects synchronization errors and is reset by software
- Supports a maximum clock of 6.8MHz (based on HCLK/2 = 54.7MHz as the SPI source clock)

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5.7.4. Auxiliary Serial Interface

The SE880 provides an auxiliary serial interface that can be configured as either a master I^2C interface or a master SPI bus. These features are implemented using either 2 or 4 of the GPIO pins on SE880. Only one of these buses may be implemented on a receiver. At start-up, the receiver automatically detects either an I^2C EEPROM or a SPI serial flash memory and sets itself appropriately. If SE880 does not detect memory of either type, the system is configured for an I^2C bus for sensor interface.

During the auto-detect process, GPIO[4:3] and GPIO[1:0] are momentarily driven high and low.

Master SPI Interface:
Non-volatile memory storage can be provided by 4Mbit serial flash memories from either SST or EON. The flash memory can store a ROM patch, both server-generated and client-generated extended ephemeris files (up to 31 days in length), satellite almanacs, crystal temperature characterization data and data logs. All of these items can be stored simultaneously on the same flash device.

Through the master SPI interface, SE880 reads and writes data at approximately 1.0Mbps, with a maximum of 1.25Mbps.

Master I^2C Interface:
This mode is the default for the receiver. It can be used to communicate with MEMS sensors such as accelerometers, magnetometers and altimeters, and with EEPROM storage devices. Some features of the interface include:

- Support for most common sensor formats (accelerometers, gyros, magnetometers, altimeters)
- upport for multiple data lengths
- Standard I^2C bus data rates of 100kbps and 400kbps
- Accepts both 64KB and 128KB EEPROMS
- 128KB EEPROMs can store server-generated EE files up to 7 days in length

Only an approved accelerometer (KIONIX part number KXTF9-4100, 3 x 3mm LGA 1.8V 3 axis accelerometer) can be used. The interrupt output of the accelerometer must be connected to GPIO4 of the SE880.

Data for the approved magnetic sensor (Aichi Steel part number AIM304, 3.5 x 4.0mm 3V 3 axis magnetometer) is output in OSP message 72.

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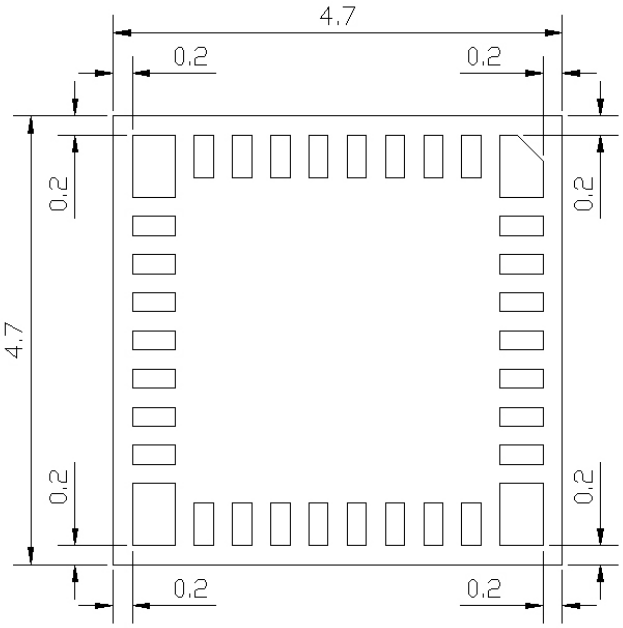
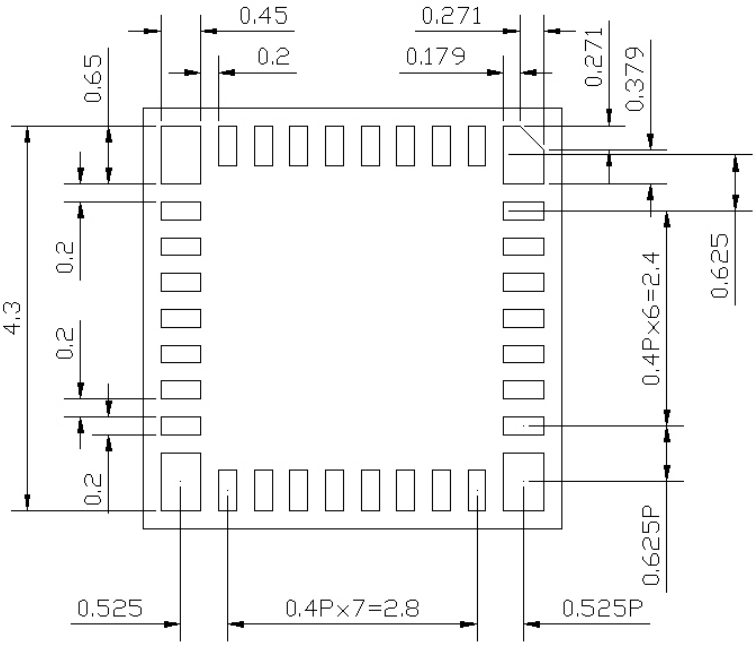
6. PCB Layout

6.1. Pins dimensions

Note: Bottom view in mm





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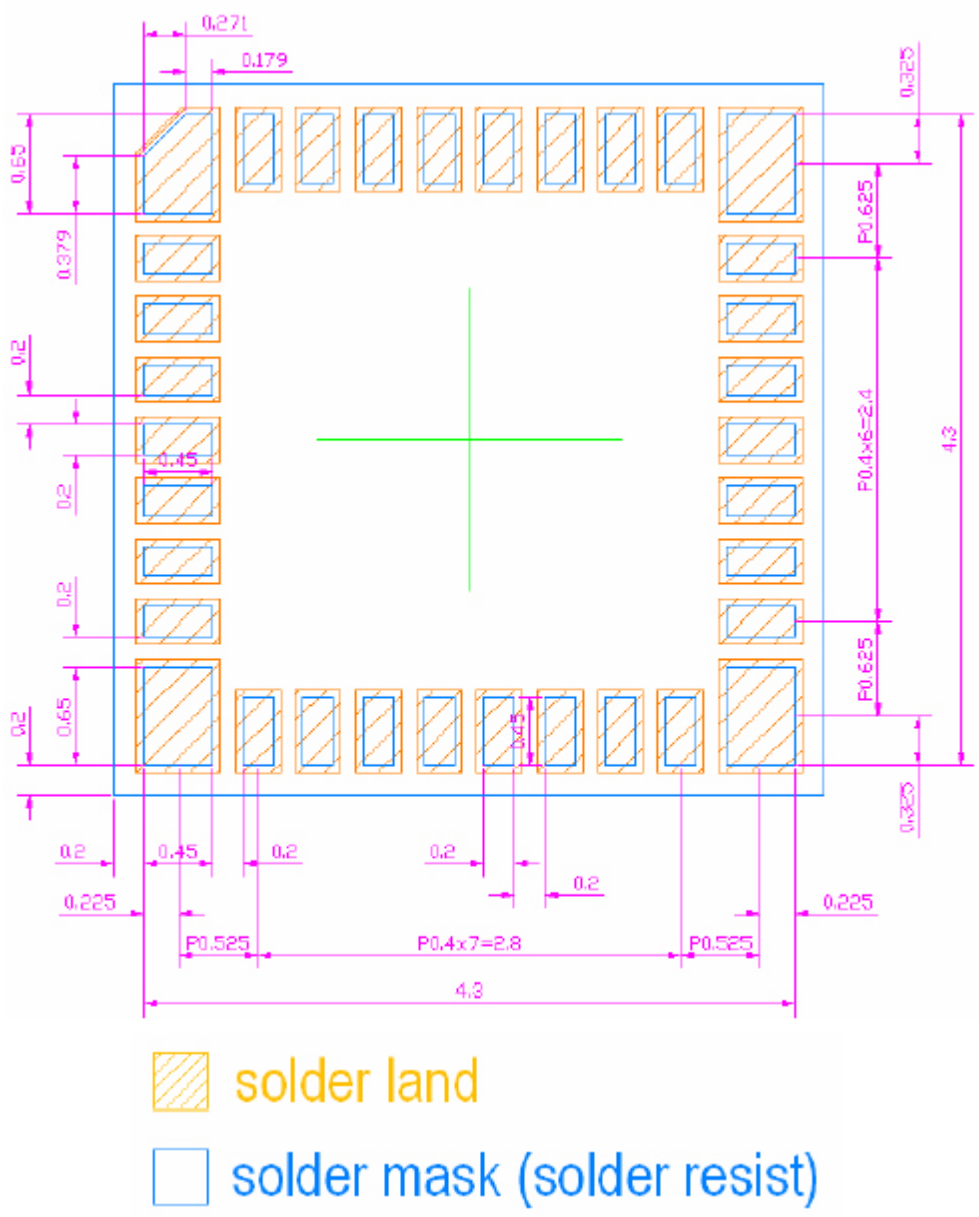
6.2. Solder Land Design for Main Mother board

Note: Top view in mm



NOTE:

The solder land is defined by solder mask opening (SMD Pads) in blue color above. The area in yellow is not the actual size of the solder land and it is governed by the PCB design rules defined by the device integrators.

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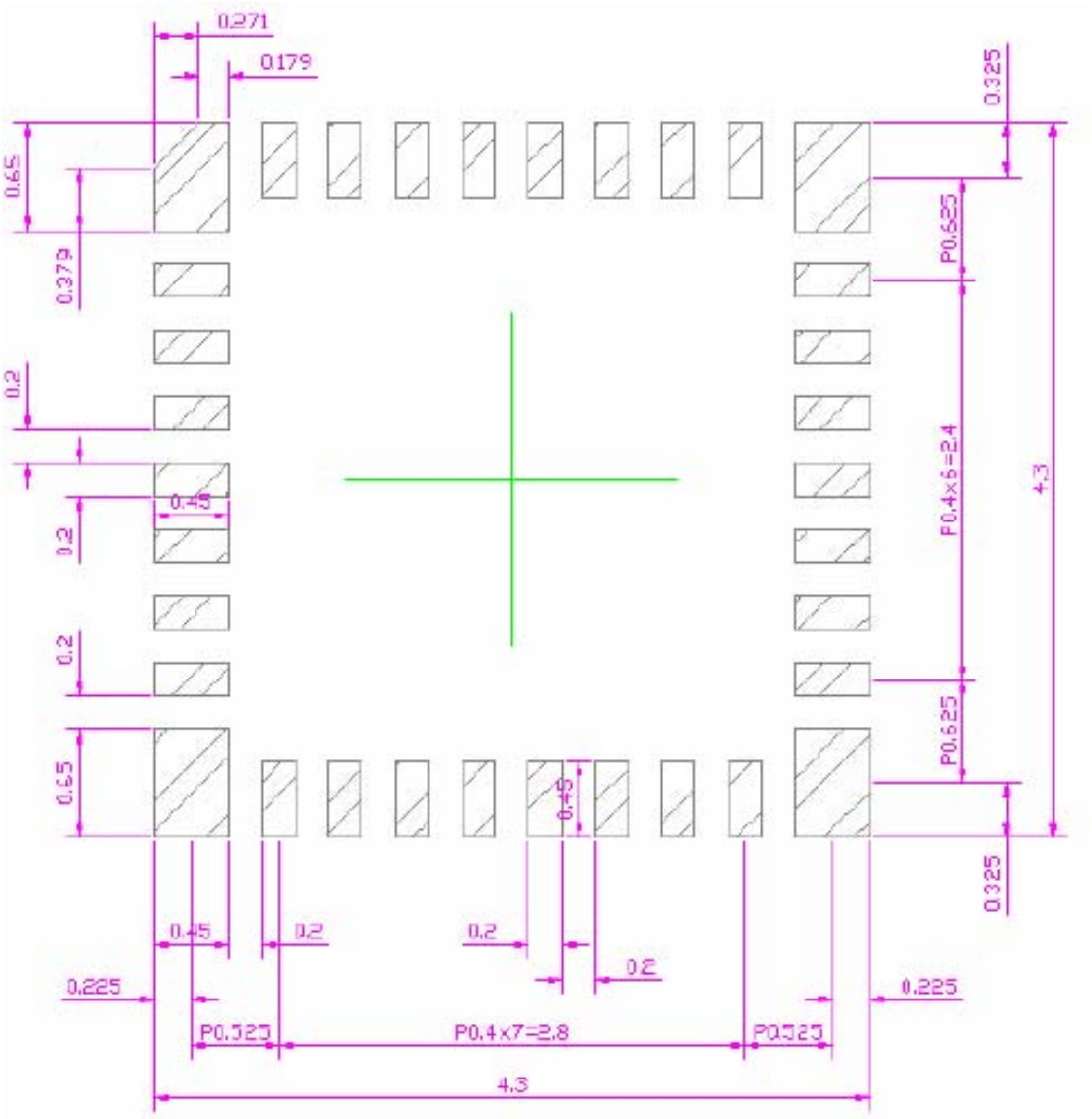
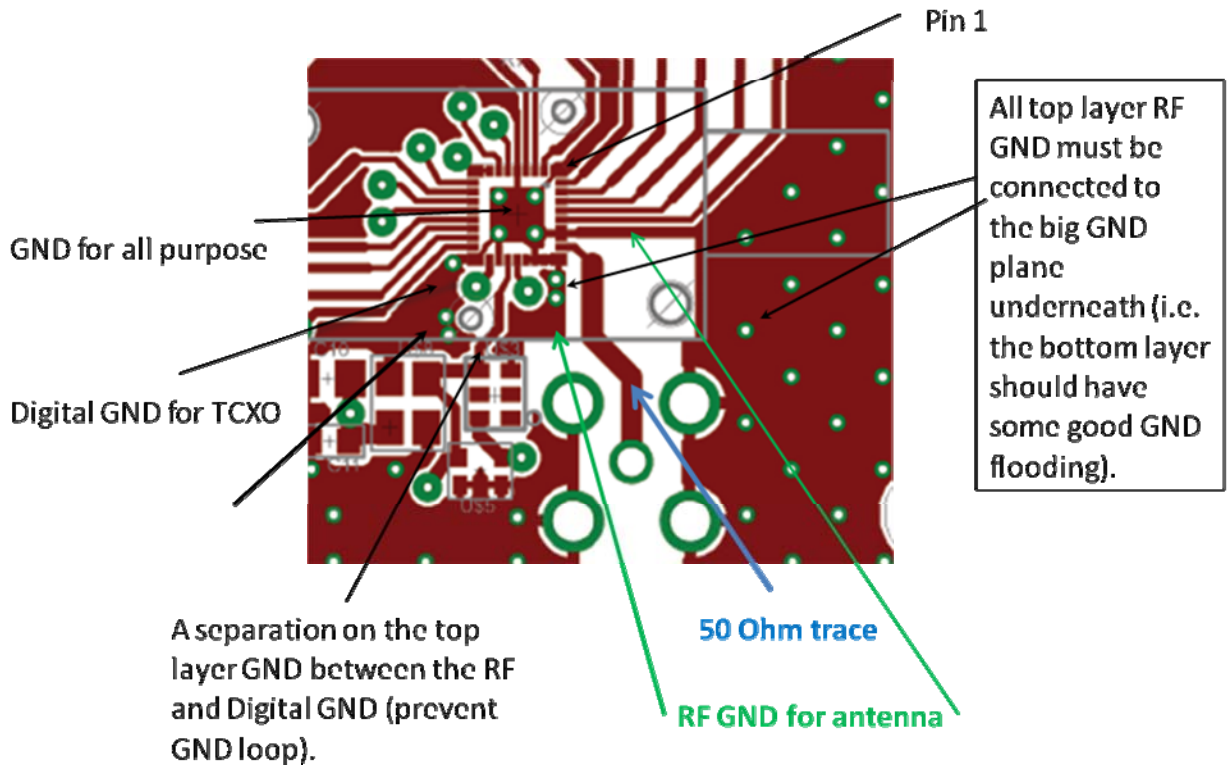
6.3. Solder Paste Stencil

Note: Top view in mm
(reference thickness : 3 mil or 0.076mm)



6.4. Layout Example for SE880 – Grounding Concept


Pin 1
All top layer RF GND must be connected to the big GND plane underneath (i.e. the bottom layer should have some good GND flooding).
GND for all purpose
Digital GND for TCXO
A separation on the top layer GND between the RF and Digital GND (prevent GND loop).
50 Ohm trace
RF GND for antenna

NOTE:

Use RF GND pin 23~26, 28 &29 for Antenna's ground.

Backside of the PCB or the next layer beneath the top signal traces should be flooded with GND plane.

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7. Antenna

7.1. Antenna Requirements

The SE880 is architected to use with passive antenna and conformal antenna design in a compact structure in which RF trace loss can be minimized by bringing the antenna close to the RF input port of the SE880 whereas RF ground is provided alongside for the completion of the antenna's grounding.

Right hand circularly polarized (RHCP) GPS antenna with center frequency at 1.575GHz should be used. A linearly polarized antenna will have 3dB loss as compared to an RHCP polarized antenna as the GPS signal is right hand circularly polarized.

Antenna Gain and RF Link Budget:
Antenna's power gain or simply gain is a key performance figure which combines the antenna's directivity and electrical efficiency. As a receiving antenna for GPS, the figure describes how well the antenna converts radio waves arriving from the space into electrical power. This gain is expressed in dBi and is different to the "gain" of an active antenna which is mostly misinterpreted during the design of a GPS receiver. The gain of an active antenna is referring to the low-noise-amplifier's gain (LNA gain) inside of the active antenna. This gain doesn't help to improve the energy conversion from the radio wave arriving from the space into electrical power.

The calibrated waveguide quality structure of SE880 brings the system noise figure consistently down to 3.5dB (NFreceiver) in LDO mode, in which about 0.4dB belongs to the implementation loss at the RF front end. The following equation can be used to calculate the sensitivities of SE880.

$$\mathbf{Sensitivity_{minimum} = -174dBm/Hz + C/No_{minimum} + NF_{receiver}}$$

The minimum carrier–to–noise ratio (C/No minimum) at the input of the quantizer of SE880 is 22dB-Hz for satellites acquisition (i.e. Cold Start sensitivity). So the cold start sensitivity of SE880 is -148.5dBm (-174+22+3.5). If an active antenna with LNA gain of 16dB and NF of 2dB is used, the sensitivity of SE880 can only be improved by 0.3dB to -148.8dBm. So the improvement to cost ratio is not significant by using an active antenna. Therefore in a compact GPS design, if there is no excessive loss due to a long lossy RF trace or a cable between the antenna and the SE880, the passive antenna's gain is the determination factor for the overall system sensitivity. For example, if the passive antenna gain is 1dBi, it brings the cold start system sensitivity to -149dBm minimum.

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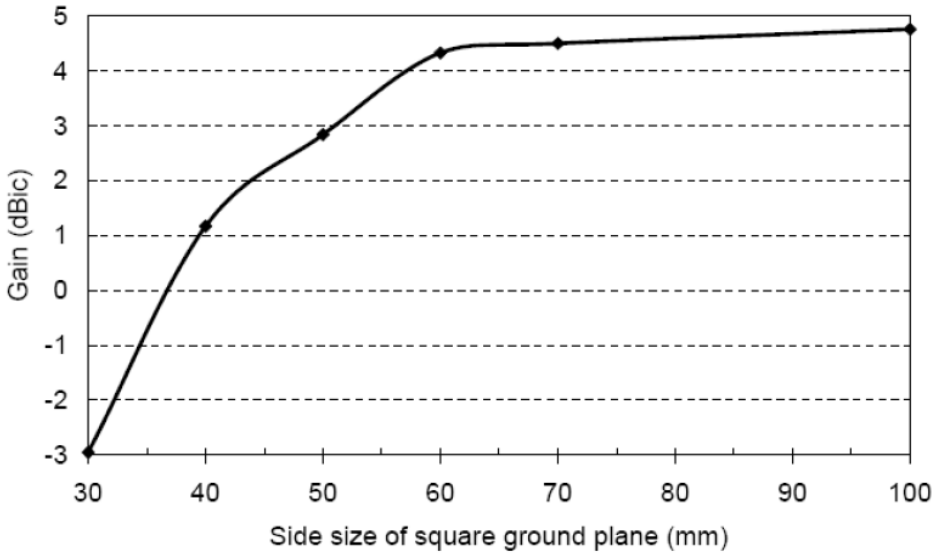
Antenna Ground:

The gain of a passive antenna is not a static number but is largely depended on the size of the ground plane. The following table shows the effect of antenna gain with variation in size for both of the antenna and ground plane.

Ceramic Patch

Antenna Size (mm)	Groundplane (mm)	Gain (dbi)
35 x 35	75 x 75	4.0
25 x 25	70 x 70	5.0
18 x 18	50 x 50	2.5
15 x 15	40 x 40	-1.0
13 x 13	40 x 40	-2.0
12.8 x 12.8	40 x 40	-2.5
12 x 12	35 x 35	-2.5
10 x 10	30 x 30	-4.0
9 x 9	30 x 30	-3.0

The following example shows the relationship of antenna gain versus ground plane size for a 25 x 25 x 4 mm ceramic patch RHCP antenna.



The ground plane requirements for different types of GPS antenna are different. It is necessary to check with the antenna's venders for the ground plane design. Other than the most commonly used ceramic patch antenna, there are helical antenna, chip antenna and printed antenna. The following example demonstrated a PCB printed antenna was designed with the SE880 by a third party developer. A similar printed antenna with other combination of passive antennas shall be included in the SE880 Reference Design Kit.

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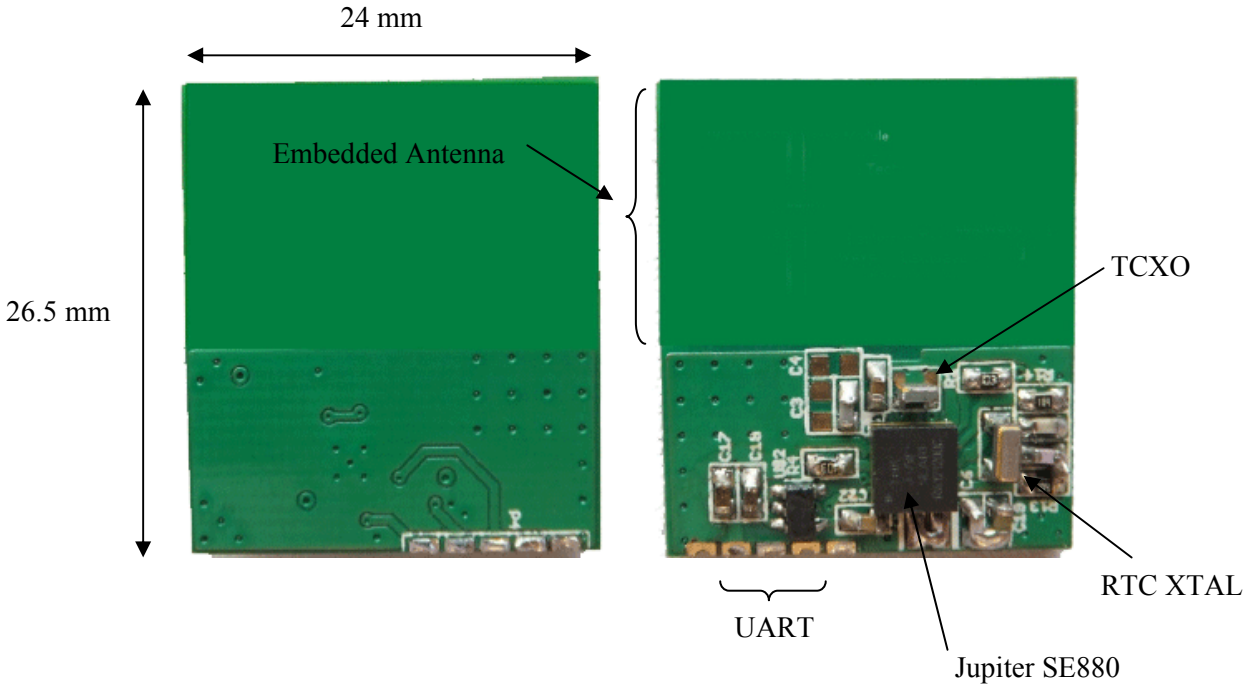
Application Example of PCB Printed Antenna



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8. Handling and soldering

8.1. ESD

The SE880 is an electrostatic discharge sensitive device and should be handled in accordance with JESD625-A requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices. The expecting handling of the SE880 during assembly and test is identical to that of a semiconductor device.

Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

8.2. Reflow

The SE880 is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, "Classification Reflow Profiles". Although IPC/JEDEC J-STD-020 allows for three reflows, the assembly process for the SE880 uses one of those profiles. Thus the SE880 is limited to two reflows.

Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

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9. Safety Recommendations

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because of the risk of disturbing external networks or devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information's are available on the European Community website:

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

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10. Document History

Revision	Date	Changes
0	2012-10-31	First Release

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